CLAIMS

We claim:

1. A method for operating a microprocessor to reduce power consumption, the microprocessor including a functional unit formed of a plurality of stages, the method comprising:

evaluating instructions to be executed to determine the operation type of each of said instructions;

producing activity indicators based upon the operation types of said instructions;

controlling the supply of current to each of said plurality of stages such that only selected stages of said plurality of stages will draw current from a power supply, the controlling being based upon activity indicators associated with each of said stages;

advancing said instructions within the microprocessor; and

executing said instructions that are within each of said selected stages.

2. A method for operating a microprocessor as recited in claim 1 wherein said microprocessor is a very long instruction word processor.

3. A method for operating a microprocessor as recited in claim 1 wherein the evaluating operates to determine whether each of said instructions is an operation instruction type or a no-operation instruction type.

4. A method for operating a microprocessor as recited in claim 3 wherein the type of instructions executed in each of said selected stages is an operation instruction type.

5. A method for operating a microprocessor as recited in claim 3 wherein the producing operates to produce a power-on activity indicator associated with operation instruction types, and a power-off activity indicator associated with no-operation instruction types.

6. A method for operating a microprocessor as recited in claim 5 wherein said selected stages are associated with power-on activity indicators, and wherein the remaining stages are associated with power-off activity indicators.

7. A method for operating a microprocessor as recited in claim 1 wherein the controlling operation further comprises:

transmitting a clock signal only to the selected stages of the functional unit.

8. A method for operating a microprocessor as recited in claim 1 further comprising repeating all of said operations for successive instructions.

9. A method for operating a microprocessor to reduce power consumption, the microprocessor including a functional unit formed of a plurality of stages, the method comprising:

evaluating instructions to determine the operation type contained within said instructions;

transmitting a null-bit to a memory device when said instructions contain a no-operation instruction, and transmitting a 1-bit to said memory device when said instructions contain an operation instruction, each of said null-bit and 1-bit being associated with a particular stage of said functional unit;

controlling the supply of current to each of said plurality of stages such that said stages of said functional unit associated with a 1-bit draw current and said stages of said functional unit associated with a null-bit do not draw current;

advancing said instructions within said microprocessor; and

executing said instructions that are within each of said stages that is associated with a 1-bit.

10. A method for operating a microprocessor as recited in claim 9 wherein said microprocessor is a very long instruction word processor.

11. A method for operating a microprocessor as recited in claim 9, wherein the controlling operation further comprises:

transmitting a clock signal to only said stages associated with a 1-bit, such that the stages associated with a null-bit do not receive a clock signal .

12. A method for operating a microprocessor as recited in claim 9 further comprising transmitting a clock signal to the memory device, the clock signal to each of said stages being transmitted after the signal to said memory device is transmitted.

13. A method for operating a microprocessor as recited in claim 9 wherein the microprocessor contains a plurality of memory devices and a plurality of functional units, each of said functional units being connected to a respective one of said plurality of memory device.

14. A method for operating a microprocessor as recited in claim 13 wherein said microprocessor is a very long instruction word processor, each instruction containing a plurality of sub-instructions, each of said sub-instructions assigned to one or more of the plurality of functional units.

15. A method for operating a microprocessor as recited in claim 9 wherein said memory device is a shift register.

16. A method for operating a microprocessor as recited in claim 9 further comprising repeating the operations for each successive instruction.

17. A microprocessor that operates in a manner that conserves power, the microprocessor comprising:

an instruction evaluation unit that evaluates a next instruction to be executed and which produces activity indicators;

a functional unit for executing instructions, the functional unit having a plurality of stages, each of said stages capable of being separately activated or deactivated based upon a respective activity indicator; and

a stage activation controller that utilizes said activity indicators and causes each of said stages to be activated or deactivated.

18. A microprocessor as recited in claim 17 wherein the microprocessor is a very long instruction word processor.

19. A microprocessor as recited in claim 17 wherein each of said stages have separate inputs for receivingcurrent, the inputs capable of being separately opened or closed, the activated stages having opened inputs and the deactivated inputs having closed inputs.

20. A microprocessor as recited in claim 17 wherein the stage activation controller is a memory unit that stores said activity indicators.

21. A microprocessor as recited in claim 20 wherein said memory unit is a register having a bit size equal to the number of stages in said functional unit, each bit location

storing a respective activity indicator which indicates whether to activate or deactivate a respective stage.

22. A microprocessor as recited in claim 17 further comprising a plurality of functional units, each of said functional units having a plurality of stages, each of said stages capable of being separately activated or deactivated based upon a respective activity indicator.

23. A microprocessor as recited in claim 22 further comprising a plurality of stage activation controllers, each of said stage activation controllers using said activity indicators to individually activate or deactivate each of said stages of a respective one of the plurality of functional units.

24. A microprocessor as recited in claim 23 further comprising a plurality of instruction evaluation units, each of said instruction evaluation units associated with a respective one of said stage activation controllers.

25. A microprocessor as recited in claim 17 further comprising a clock circuit, said clock circuit supplying a stage activation controller clock pulse to said stage activation controller and a functional unit clock pulse to said functional unit, said functional unit clock pulse being time-delayed with respect to said stage activation controller clock pulse.

26. A microprocessor that operates in a manner that conserves power, the microprocessor comprising:

an instruction evaluation unit that evaluates a next instruction to be executed and which produces activity indicators;

a functional unit for executing instructions, said functional unit having a plurality of stages, each of said stages capable of being separately activated or deactivated based upon a respective activity indicator; and

a stage activation controller that utilizes said activity indicators and causes each of said stages of said functional unit to be individually activated or deactivated.

27. A microprocessor as recited in claim 26 further comprising:

a clock circuit for supplying clock pulses to each stage of said functional unit and to said stage activation controller; and

an instruction register containing said next operation to be executed by said functional unit.

28. A microprocessor as recited in claim 26 wherein the microprocessor is a very long instruction word processor.

29. A microprocessor as recited in claim 26 wherein said clock circuit has a delay circuit that causes the pulse supplied to said functional stages to be transmitted at a time slightly after the transmission of the pulse to said stage activation controller.

30. A microprocessor as recited in claim 26 wherein each of said stages have separate inputs for receiving a clock signal, the inputs capable of being separately opened or closed, the activated stages having opened inputs and the deactivated inputs having closed inputs.

31. A microprocessor as recited in claim 26 wherein said stage activation controller is a memory unit that stores said activity indicators.

32. A microprocessor as recited in claim 31 wherein said memory unit is a register having a bit size equal to the number of stages in said functional unit, each bit location storing a respective activity indicator which indicates whether to activate or deactivate a respective stage.

33. A microprocessor as recited in claim 1 further comprising a plurality of functional units, each of said plurality of functional units having a plurality of stages, each of said stages capable of being separately activated or deactivated based upon a respective activity indicator.

34. A microprocessor as recited in claim 33 further comprising a plurality of stage activation controllers, each of said stage activation controllers using said activity indicators to activate or deactivate individual stages within a respective one of the plurality of functional units.

35. A microprocessor as recited in claim 33 wherein said microprocessor is a very long instruction word processor.

36. A microprocessor as recited in claim 35 further comprising a plurality of instruction evaluation units, each of said instruction evaluation units associated with a respective one of said stage activation controllers.

37. A computer system that operates in a manner that reduces power consumption, comprising:

a microprocessor wherein the microprocessor includes,

an instruction evaluation unit that evaluates a next instruction to be executed and which produces activity indicators;

a functional unit for executing instructions, the functional unit having a plurality of stages, each of said stages capable of being separately activated or deactivated based upon a respective one of the activity indicators; and

a stage activation controller that utilizes said activity indicators and causes each of said stages to be activated or deactivated;

a main memory for storing data, including instructions executable on microprocessor;

at least one I/O device; and

at least one bus supporting transfer of data between components of the computer system.

38. A computer system as recited in claim 37 wherein said microprocessor is a very long instruction word processor.